

Copper Electroplating Process for Sum-Half-Micron ULSI Structures

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Abstract

The demand for copper metallization increases as the need grows for downward scaling of devices to achieve high conductivity for high circuit speeds, high packing densities, and low power dissipation. The damascene process for copper-based interconnection is particularly well-suited to blanket metal deposition, followed by chemical-mechanical polishing. Electroplating is an important means of achieving the blanket deposition.

We have utilized electroplating technology to produce low resistance copper (< 1.9 micro-ohm-cm) interconnects in sub-half-micron ULSI patterns having aspect ratios over 2:1. The use of a pulsed-voltage plating technique allows for enhanced filling capability without voids.

Samples of 150 mm diameter were patterned by standard photolithographic techniques in the dielectric layer, and sputtered with a Ta or TiN barrier layer, followed by a copper seed layer. Pulsed-voltage electroplating deposits about 2 microns of copper uniformly (1 sigma $< 5\%$) over the surface. The electroplated copper has low levels of impurities (as compared to other copper deposition methods), excellent adhesion, excellent step coverage, and rates comparable to other deposition methods. The plating bath chemistry utilizing copper sulfate and sulfuric acid is particularly simple, robust, and stable for long periods of time, with low environmental impact. Furthermore, the plating tool is low in cost and maintenance as compared to other copper deposition techniques. We present details of the electroplating equipment, and data on the filling characteristics of the copper metallization which prevent void formation and reduce contact resistance.

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